

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization  
International Bureau



(43) International Publication Date  
19 September 2002 (19.09.2002)

PCT

(10) International Publication Number  
**WO 02/073620 A2**

(51) International Patent Classification<sup>7</sup>: **G11C 11/16** (74) Agents: BRADEN, Stanton C. et al.; Siemens Corporation - Intellectual Property Dept., 186 Wood Ave. South, Iselin, NJ 08830 (US).

(21) International Application Number: PCT/US02/03040 (81) Designated States (*national*): CN, JP, KR.

(22) International Filing Date: 24 January 2002 (24.01.2002) (84) Designated States (*regional*): European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR).

(25) Filing Language: English (26) Publication Language: English

(30) Priority Data:  
60/263,910 24 January 2001 (24.01.2001) US  
09/836,817 17 April 2001 (17.04.2001) US

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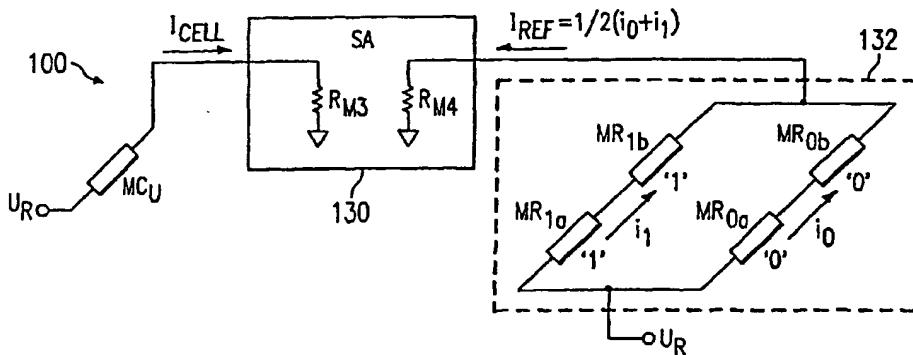
Published:

— without international search report and to be republished upon receipt of that report

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

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(54) Title: REFERENCE FOR MRAM CELL



WO 02/073620 A2

(57) Abstract: A reference circuit (132) for an MRAM array, including logic "1" reference MRAM cells (MR<sub>1a</sub>) and (MR<sub>1b</sub>) coupled in parallel with logic "0" reference MRAM cells (MR<sub>0a</sub>) and (MR<sub>0b</sub>). The reference current (I<sub>ref</sub>) is coupled to a measurement resistor (R<sub>m</sub>) of a sense amplifier (130) which is adapted to determine the logic state of an unknown memory cell MC<sub>u</sub>.

**Reference for MRAM Cell**

This patent claims the benefit of U.S. Provisional Patent Application Serial No. 60/263,910, filed January 24, 2001, which is incorporated herein by reference.

**TECHNICAL FIELD**

The present invention relates generally to the fabrication of semiconductor devices, and more particularly to magnetic random access memory (MRAM) devices.

**BACKGROUND OF THE INVENTION**

Semiconductors are used for integrated circuits for electronic applications, including radios, televisions, cell phones, and personal computing devices, as examples. One type of semiconductor device is a semiconductor storage device, such as a dynamic random access memory (DRAM) and flash memory, which use an electron charge to store information.

A more recent development in memory integrated circuit devices involves spin electronics, which combines semiconductor technology and magnetics. The spin of an electron, rather than the charge, is used to indicate the presence of a "1" or "0". One such spin electronic device is a magnetic random-access memory (MRAM), which includes conductive lines positioned perpendicular to one another in different metal layers, the conductive lines sandwiching a magnetic stack. The place where the conductive lines intersect is called a cross-point. A current flowing through one of the conductive lines generates a magnetic field around the conductive line and orients the magnetic polarity into a certain direction along the wire or conductive line. A current flowing through the other conductive line induces the magnetic field and can partially turn the magnetic polarity, also. Digital information, represented as a "0" or "1", is stored in the alignment of magnetic moments. The resistance of the magnetic component depends on the moment's alignment. The stored state is read from the element by detecting the component's resistive state. A memory cell may be constructed

by placing the conductive lines and cross-points in a matrix structure or array having rows and columns.

An advantage of MRAMs compared to traditional semiconductor memory devices such as DRAMs is that MRAMs provide a non-volatile memory. For example, a personal computer (PC) utilizing MRAMs would not have a long "boot-up" time as with conventional PCs that utilize DRAMs. Also, an MRAM has the capability of remembering the stored data.

In order to read an MRAM storage cell, it is necessary to have a reference circuit so that the stored information can be sensed. In prior art MRAM cells, the reference circuit is located in a remote circuit, away from the MRAM array area, made of materials different from the MRAM storage cells, such as N-type field effect transistors (N-FET's) and P-FET's, as examples. This is disadvantageous because process flow materials and methods change differently for different devices during the process flow. These variables introduce fluctuations that can deleteriously impact the reference current generated, resulting in the incorrect reading of logic states of the MRAM memory cells.

What is needed in the art is an MRAM reference circuit design capable of accurately reading the logic state of MRAM storage cells.

#### SUMMARY OF THE INVENTION

The present invention achieves technical advantages as a reference circuit and method thereof for an MRAM device, having logic "1" and logic "0" MRAM storage cells coupled in parallel and being adapted to supply a reference current for a sensing amplifier of an MRAM array to determine the logic state of MRAM cells in the MRAM array.

Disclosed is a reference circuit for an MRAM array, comprising at least one MRAM storage cell having a logic "1" stored therein, and at least one MRAM storage cell having a logic "0" stored therein coupled to the logic "1" MRAM storage cell, wherein the reference circuit is adapted to supply a

reference current for a sensing amplifier of the MRAM array to determine the logic state of MRAM cells in the array.

Further disclosed is a reference circuit for an MRAM array, comprising a first logic "1" storage cell having a first end and a second end, a second logic "1" storage cell having a first end and a second end coupled in series at the first end to the second end of the first logic "1" storage cell, a first logic "0" storage cell having a first end and a second end coupled at the first end to the first logic "1" storage cell first end, and a second logic "0" storage cell having a first end and a second end coupled in series at the first end to the second end of the first logic "0" storage cell, the second logic "0" storage cell second end being coupled to the second logic "1" storage cell second end, wherein the reference circuit is adapted to supply a reference current for a sensing amplifier of the MRAM array to determine the logic state of MRAM cells in the array.

Also disclosed a method of generating a reference current for a sensing amplifier of an MRAM device, the MRAM device comprising a plurality of storage cells arranged in an array, each storage cell comprising a logic state, comprising supplying a reference current, wherein the reference current comprises half of the current through at least one logic "1" MRAM storage cell and half the current through at least one logic "0" MRAM storage cell, wherein the logic state of an MRAM storage cell in the array is determinable by comparing the MRAM storage cell current and the reference current.

Advantages of the invention include providing a reference circuit having MRAM cells in the same type of array or same array as the MRAM cells to be read, so that the reference MRAM cells have been exposed to the same processing parameters and fluctuations as the MRAM cells being read. This is advantageous because the material and process related deviations and fluctuations are the same for the reference MRAM cells and the unknown MRAM cells being read, resulting in

a more accurate reading of the unknown MRAM cells. Another advantage of the present invention is that half the current or midpoint between a logic "1" and a logic "0" memory cell is used as a reference current, resulting in the ability to accurately read whether the resistance of the MRAM storage cell is a logic "0" or a logic "1".

**BRIEF DESCRIPTION OF THE DRAWINGS**

The above features of the present invention will be more clearly understood from consideration of the following descriptions in connection with accompanying drawings in which:

Figure 1 shows a perspective view of an MRAM array having bitlines orthogonal to wordlines, sandwiching and electrically coupled to magnetic stacks that are adapted to store a logic "1" or "0";

Figure 2 illustrates an example of a prior art schematic for reading an MRAM storage cell in an array, including a sense amplifier and a reference current circuit;

Figure 3 shows a schematic of an embodiment of the reference circuit for an MRAM device in accordance with the present invention;

Figure 4 illustrates another embodiment of the reference circuit in accordance with the present invention;

Figure 5 illustrates an embodiment of the present invention in which the reference circuit is located in an separate MRAM array; and

Figure 6 illustrates an implementation of the present invention wherein the reference circuit is located in the same MRAM array as the memory storage cells being read.

Corresponding numerals and symbols in the different figures refer to corresponding parts unless otherwise indicated. The figures are drawn to clearly illustrate the relevant aspects of the preferred embodiments and are not necessarily drawn to scale.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Prior art MRAM array reference circuits will be discussed, followed by a description of preferred embodiments and some advantages of the present invention.

Figure 1 illustrates a perspective view of a prior art MRAM 10 having bitlines 12 located orthogonal to wordlines 14 in adjacent metallization layers. Magnetic stacks 16 are positioned between the bitlines 12 and wordlines 14 adjacent and electrically coupled to bitlines 12 and wordlines 14. Magnetic stacks 16 preferably comprise multiple layers, including a soft layer 18, a tunnel layer 20, and a hard layer 22, for example. Soft layer 18 and hard layer 22 preferably comprise a plurality of magnetic metal layers, for example, eight to twelve layers of materials such as PtMn, CoFe, Ru, and NiFe, as examples. Tunnel layer 20 comprises a dielectric such as Al<sub>2</sub>O<sub>3</sub>, for example. A logic state is storable in the soft layer 18 of the magnetic stacks 16 located at the junction of the bitlines 12 and wordlines 14 by running a current in the appropriate direction within the bitlines 12 and wordlines 14, which changes the resistance of the magnetic stacks 16.

In order to read the logic state stored in the soft layer 18 of the magnetic stack 16, a schematic such as the one shown in Figure 2, including a sense amplifier (SA) 30, is used to determine the logic state stored in an unknown memory cell MC<sub>u</sub>. A reference voltage U<sub>R</sub> is applied to one end of the unknown memory cell MC<sub>u</sub>. The other end of the unknown memory cell MC<sub>u</sub> is coupled to a measurement resistor R<sub>m1</sub>. The other end of the measurement resistor R<sub>m1</sub> is coupled to ground. The current running through the unknown memory cell MC<sub>u</sub> is equal to current I<sub>cell</sub>. A reference circuit 32 supplies a reference current I<sub>ref</sub> that is run into measurement resistor R<sub>m2</sub>. The other end of the measurement resistor R<sub>m2</sub> is coupled to ground, as shown.

The sense amplifier 30 comprising a comparator, for example, is adapted to compare currents I<sub>cell</sub> and I<sub>ref</sub> because measurement resistors R<sub>m1</sub> and R<sub>m2</sub> are equal. In this manner,

the sense amplifier 30 can detect the logic state of the unknown memory cell MC<sub>u</sub>. For example, a high ohmic state or "1" shows typically 20% higher resistance than the detected resistance of a memory cell MC<sub>u</sub> having a "0" or low ohmic state, e.g., 12 kΩ for an ohmic "1" state and 10 kΩ for an ohmic "0" state.

A problem with the circuit shown in the prior art drawing of Figure 2 is that the reference current I<sub>ref</sub> is generated away from the MRAM bit cell array in a circuit or IC different from the memory array of the MRAM. This is undesirable, because fluctuations in the materials, processing and manufacturing of the memory array containing the unknown memory cell MC<sub>u</sub> may cause a need for a varied reference current I<sub>ref</sub>. Reference generator 32 is always device dependent and temperature dependent, and usually does not have the same performance as an actual memory cell MC<sub>u</sub>. Also, the memory cell MC<sub>u</sub> behaves differently than other circuits located away from the MRAM array.

The present invention achieves technical advantages by using MRAM cells for creating a reference current. This is advantageous because the reference MRAM cells are exposed to the same material and processing changes and fluctuations during manufacturing, and thus have a better match of various material and electrical properties as the MRAM cells MC<sub>u</sub> being read.

The MRAM memory cells described herein may also be referred to as magnetic stacks, or magnetic tunnel junction (MTJ) stacks.

Figure 3 illustrates a schematic 100 of a preferred embodiment of the present invention. A sense amplifier 130 comprises a first measurement resistor R<sub>m3</sub> and a second measurement resistor R<sub>m4</sub>. Sense amplifier 130 preferably comprises a comparator, for example. One end of the first and second measurement resistors RM<sub>3</sub> and RM<sub>4</sub> is coupled to ground. The first measurement resistor R<sub>m3</sub> is coupled at the other end to an unknown memory cell MC<sub>u</sub>. The unknown memory cell MC<sub>u</sub>

comprises a memory cell within a MRAM array for which the logic state is desired to be read and determined. For example, a logic state was previously stored within memory cell MC<sub>u</sub>, and now this logic state will be retrieved by the SA 130 utilizing the reference current I<sub>ref</sub> generated by the reference circuit 132. The unknown memory cell MC<sub>u</sub> is also coupled at the other end to a reference voltage U<sub>r</sub>. Reference voltage U<sub>r</sub> preferably is 0.5 volts, although reference voltage U<sub>r</sub> may range from 0.1 to 5 volts, as examples. The current flowing through the unknown memory cell MC<sub>u</sub> is equal to current I<sub>cell</sub>.

In accordance with a preferred embodiment, the reference circuit 132 that generates the reference current I<sub>ref</sub> comprises two MRAM memory cells MR<sub>1a</sub>/MR<sub>1b</sub> having a logic "1" stored therein in series with two MRAM cells MR<sub>0a</sub>/MR<sub>0b</sub> having a logic "0" stored therein, as shown. A first logic "1" MRAM cell MR<sub>1a</sub> is coupled in series with a second logic "1" MRAM cell MR<sub>1b</sub>. A first logic "0" MRAM cell MR<sub>0a</sub> is coupled in series with a second logic "0" MRAM cell MR<sub>0b</sub>. The series logic "1" MRAM cells MR<sub>1a</sub>/MR<sub>1b</sub> are coupled in parallel with the series logic "0" MRAM cells MR<sub>0a</sub>/MR<sub>0b</sub>, and the parallel circuit 132 is coupled at one end to one end of the second measurement resistor R<sub>m4</sub> of the sense amplifier 130. The other end of the parallel circuit 132 is coupled to reference voltage U<sub>r</sub>, the reference voltage U<sub>r</sub> being the same reference voltage U<sub>r</sub> on the MRAM array comprising the unknown memory cell MC<sub>u</sub> for which the logic state is being read. The reference circuit 132 generates a current I<sub>ref</sub> that is equal to:

$$I_{ref} = \frac{1}{2} (i_0 + i_1);$$

where i<sub>0</sub> is equal to the current through the series logic "0" MRAM cells MR<sub>0a</sub> and MR<sub>0b</sub>, and the current i<sub>1</sub> is equal to the current through series logic "1" MRAM cells MR<sub>1a</sub> and MR<sub>1b</sub>.

Another preferred embodiment of the present invention is shown in the schematic 200 of Figure 4. In this embodiment,

the second measurement resistor  $R_{m4}$  of the sense amplifier 230 is coupled to one logic "1" MRAM cell  $MR_1$  that is coupled in parallel with one logic "0" MRAM cell  $MR_0$ . The parallel reference circuit 232 created by the logic "1" MRAM cell  $MR_1$  and the logic "0" MRAM cell  $MR_0$  coupled in parallel is coupled at one end to the sense amplifier 230 second measurement resistor  $R_{m4}$ , and is coupled at the other end to a signal equivalent to 0.5 times the reference voltage  $U_r$ . Again, the reference current  $I_{ref}$  is equal to:

$$I_{ref} = \frac{1}{2} (i_1 + i_0);$$

where current  $i_0$  is equal to the current flowing through logic "0" MRAM cell  $MR_0$ , and current  $i_1$  is equal to the current flowing through logic "1" MRAM cell  $MR_1$ .

A parallel reference circuit 132/232 in accordance with the present invention including at least one logic "1" MRAM cell and at least one logic "0" MRAM cell coupled in parallel produces a reference current  $I_{ref}$  that comprises the mid-point current between a logic "0" and a logic "1" MRAM cell. Depending on the logic state of the unknown memory element  $MC_u$ , a large or small amount of current  $I_{cell}$  will flow through the unknown memory cell  $MC_u$ . In order to detect the correct stored information in the unknown memory element  $MC_u$ , the SA 130/230 compares the midpoint value  $I_{ref}$  generated by the reference circuit 100/200 of the present invention to the current  $I_{cell}$ .

Figure 5 illustrates the use of the schematic 200 in an implementation where the logic "1" and logic "0" MRAM cells  $MR_1$  and  $MR_0$  of the schematic in Figure 4 are used to generate the reference current  $I_{ref}$  for sense amplifier 230 in an MRAM array 240 that is away from the MRAM array 250 containing the unknown memory cell  $MC_u$ . The MRAM array 250 includes wordlines 252 and bitlines 254 that are used to address each of the memory cells in the array including the unknown memory cell  $MC_u$ . Similarly, the MRAM array 240 that includes the reference MRAM cells  $MR_1$  and  $MR_0$  in accordance with the present invention

also includes wordlines 242 and bitlines 244 for addressing the various MRAM storage cells of the MRAM array 240 used for generating the reference current  $I_{ref}$ . Because the reference current  $I_{ref}$  is generated by two MRAM cells  $MR_1$  and  $MR_0$  that have the same materials and manufacturing process exposure as the unknown memory cell  $MC_u$  in the MRAM array 250, a more accurate reading of the resistive state of the unknown memory cell  $MC_u$  may be attained, therefore resulting in a more accurate determination of the logic state of the unknown memory cell  $MC_u$ . Sense amplifier 230 compares currents  $I_{cell}$  and  $I_{ref}$  to determine the logic state of the unknown memory cell  $MC_u$ .

Figure 6 illustrates an implementation of the reference circuit 100 shown in Figure 3, where the reference MRAM cells  $MR_{1a}$ ,  $MR_{1b}$ ,  $MR_{0a}$ , and  $MR_{0b}$  reside on the same MRAM array 350 as the unknown memory cell  $MC_u$  for which the resistive/logic state is being read and determined. Each dark circle in the array 100 represents an MRAM cell, and the grey circle represents the unknown memory cell  $MC_u$ . The reference current  $I_{ref}$  is generated by reference MRAM cells  $MR_{1a}$ ,  $MR_{1b}$ ,  $MR_{0a}$ , and  $MR_{0b}$ . The current  $I_{cell}$  flows from unknown memory cell  $MC_u$  to SA 330. The sense amplifier 330 is adapted to compare currents  $I_{ref}$  and  $I_{cell}$  to determine the logic state of  $MC_u$ . Because reference current  $I_{ref}$  is generated by MRAM reference cells  $MR_{1a}$ ,  $MR_{1b}$ ,  $MR_{0a}$ , and  $MR_{0b}$  on the same integrated circuit or MRAM array 350 as the unknown memory cell  $MC_u$ , a more accurate determination of the unknown memory cell  $MC_u$  logic state can be made by the sense amplifier 330, in accordance with the present invention.

In order to write to the reference cells  $MR_{1a}$ ,  $MR_{1b}$ ,  $MR_{0a}$ , and  $MR_{0b}$  in Figure 6, conductive lines below and above the reference cells  $MR_{1a}$ ,  $MR_{1b}$ ,  $MR_{0a}$ , and  $MR_{0b}$  are used, e.g. wordlines and bitlines in M1 and M4 metallization layers, for example.

Although Figure 5 illustrates an implementation of the reference circuit 200 shown in Figure 4 in a different MRAM array 240, similarly, the reference circuit 200 shown in

Figure 4 may be implemented within the same MRAM array 350 as the unknown memory cell MC<sub>u</sub> for which the logic state is being determined, not shown. Likewise, the reference circuit 100 shown in Figure 3 may be implemented in an MRAM array 240 away from the MRAM array 250 containing the unknown memory cell MC<sub>u</sub>, as shown in Figure 5.

The present invention achieves technical advantages as a reference circuit 132/232 comprising MRAM cells MR<sub>0</sub>, MR<sub>1</sub>, MR<sub>0a</sub>, MR<sub>0b</sub>, MR<sub>1a</sub>, and MR<sub>1b</sub> that are located either on the memory array being read, or on a different memory array. Because the reference current I<sub>ref</sub> in the present invention is generated by MRAM cells MR<sub>1</sub>, MR<sub>0</sub>, MR<sub>1a</sub>, MR<sub>1b</sub>, MR<sub>0a</sub>, and MR<sub>0b</sub>, the resistances of the reference circuits 132 and 232 are matched more closely to the resistance of unknown MRAM cell MC<sub>u</sub>, resulting in a more accurate reading of the logic state of the unknown memory cell MC<sub>u</sub>. Any material or process fluctuations or deviations are shared by the MRAM array unknown memory cell MC<sub>u</sub> and the MRAM reference cells used in the parallel circuits 132 and 232 used to generate the reference current I<sub>ref</sub>. Using a reference current I<sub>ref</sub> that comprises the mid-point current between a logic "0" and a logic "1" MRAM cell provides a more accurate reading of unknown memory cells MC<sub>u</sub>.

While the invention has been described with reference to illustrative embodiments, this description is not intended to be construed in a limiting sense. Various modifications in combinations of the illustrative embodiments, as well as other embodiments of the invention, will be apparent to persons skilled in the art upon reference to the description. In addition, the order of process steps may be rearranged by one of ordinary skill in the art, yet still be within the scope of the present invention. It is therefore intended that the appended claims encompass any such modifications or embodiments. Moreover, the scope of the present application is not intended to be limited to the particular embodiments of the process, machine, manufacture, composition of matter, means, methods and steps described in the specification.

Accordingly, the appended claims are intended to include within their scope such processes, machines, manufacture, compositions of matter, means, methods, or steps.

What is claimed is:

1. A reference circuit for a magnetic random access memory (MRAM) array, comprising:
  - at least one MRAM storage cell having a logic "1" stored therein; and
    - at least one MRAM storage cell having a logic "0" stored therein coupled to the logic "1" MRAM storage cell, wherein the reference circuit is adapted to supply a reference current for a sensing amplifier of the MRAM array to determine the logic state of MRAM cells in the array.
2. The reference circuit according to Claim 1, wherein a current through the logic "1" MRAM storage cell is equal to  $i_1$ , a current through the logic "0" MRAM storage cell is equal to  $i_0$ , and the reference current is approximately equal to  $\frac{1}{2} (i_1 + i_0)$ .
3. The reference circuit according to Claim 2, comprising exactly one logic "1" MRAM storage cell and exactly one logic "0" MRAM storage cell, wherein the logic "1" and logic "0" MRAM storage cells are coupled together in parallel, wherein one end of the parallel storage cells is coupleable to a reference voltage equal to half a reference voltage for the MRAM array, and wherein the other end of the parallel storage cells is coupleable to the MRAM array sensing amplifier.
4. The reference circuit according to Claim 2, comprising:
  - two logic "1" storage cells coupled together in series;
  - two logic "0" storage cells coupled together in series, the two series logic "0" storage cells being coupled in parallel to the two logic "1" storage cells, wherein one end of the parallel storage cells are coupled to a reference voltage equal to a reference voltage for the MRAM array, and wherein the other end of the parallel storage cells is coupleable to the MRAM array sensing amplifier.

5. The reference circuit according to Claim 1, wherein the reference circuit storage cells are part of the MRAM array.

6. The reference circuit according to Claim 1, wherein the reference circuit storage cells are part of an MRAM array different from the MRAM array for which the reference current is being generated.

7. A reference circuit for a magnetic random access memory (MRAM) array, comprising:

a first logic "1" storage cell having a first end and a second end;

a second logic "1" storage cell having a first end and a second end, the second logic "1" storage cell being coupled in series at the first end to the second end of the first logic "1" storage cell;

a first logic "0" storage cell having a first end and a second end, the first logic "0" storage cell being coupled at the first end to the first logic "1" storage cell first end; and

a second logic "0" storage cell having a first end and a second end, the second logic "0" storage cell being coupled in series at the first end to the second end of the first logic "0" storage cell, the second logic "0" storage cell second end being coupled to the second logic "1" storage cell second end, wherein the reference circuit is adapted to supply a reference current for a sensing amplifier of the MRAM array to determine the logic state of MRAM cells in the array.

8. The reference circuit according to Claim 7, wherein a current through the first and second logic "1" MRAM storage cells is equal to  $i_1$ , a current through the first and second logic "0" MRAM storage cell is equal to  $i_0$ , and the reference current is approximately equal to  $\frac{1}{2} (i_1 + i_0)$ .

9. The reference circuit according to Claim 8, wherein the second logic "1" MRAM storage cell second end and the second logic "0" MRAM storage cell second end are coupled to a reference voltage equal to the reference voltage for the MRAM array, and wherein the first logic "1" MRAM storage cell first end and the first logic "0" MRAM storage cell first end are coupleable to the MRAM array sensing amplifier.

10. The reference circuit according to Claim 9, wherein the reference circuit storage cells are part of the MRAM array.

11. The reference circuit according to Claim 9, wherein the reference circuit storage cells are part of an MRAM array different from the MRAM array for which the reference current is being generated.

12. A method of generating a reference current for a sensing amplifier of a magnetic random access memory (MRAM) device, the MRAM device comprising a plurality of storage cells arranged in an array, each storage cell comprising a logic state, comprising:

supplying a reference current, wherein the reference current is a function of the current through at least one logic "1" MRAM storage cell and at least one logic "0" MRAM storage cell, wherein the logic state of an MRAM storage cell in the array is determinable by comparing the MRAM storage cell current and the reference current.

13. The method according to Claim 12, wherein the reference current comprises half of the current through at least one logic "1" MRAM storage cell and half the current through at least one logic "0" MRAM storage cell.

14. The method according to Claim 12, wherein supplying a reference current comprises:

coupling a first end of an MRAM storage cell having a logic "1" stored therein to the sensing amplifier;

coupling a first end of an MRAM storage cell having a logic "0" stored therein to the logic "1" MRAM storage cell first end and the sensing amplifier; and

coupling the second ends of the logic "1" and logic "0" MRAM storage cells to a reference voltage.

15. The method according to Claim 14, wherein the reference voltage is equal to half a reference voltage for the MRAM array.

16. The method according to Claim 14, wherein the reference circuit storage cells are part of the MRAM array.

17. The method according to Claim 14, wherein the reference circuit storage cells are part of an MRAM array different from the MRAM array for which the reference current is being generated.

18. The method according to Claim 12, wherein supplying a reference current comprises:

providing a first logic "1" storage cell having a first end and a second end;

coupling a second logic "1" storage cell having a first end and a second end at the first end to the second end of the first logic "1" storage cell;

coupling a first logic "0" storage cell having a first end and a second end at the first end to the first logic "1" storage cell first end and to a reference voltage of the MRAM array;

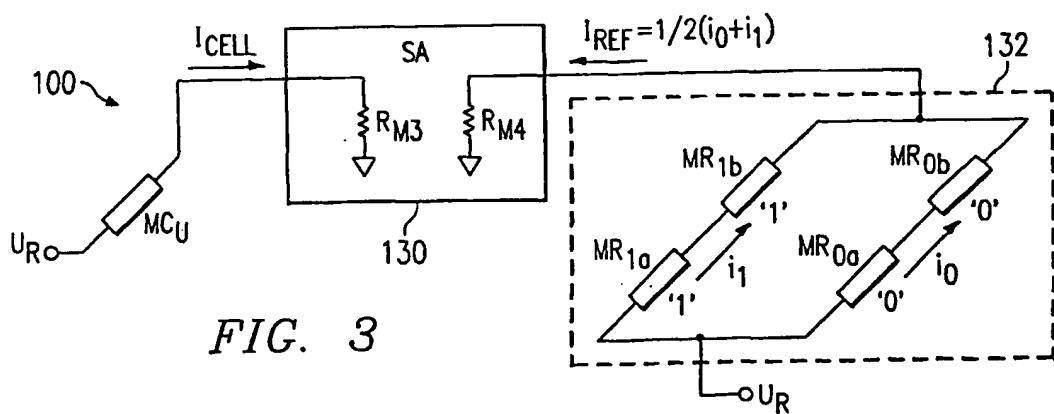
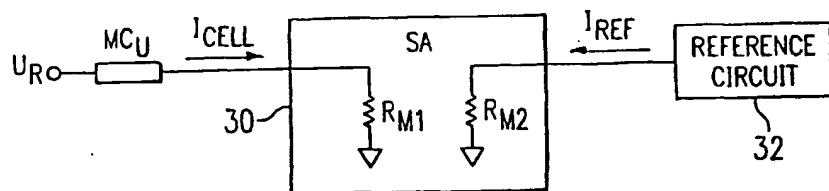
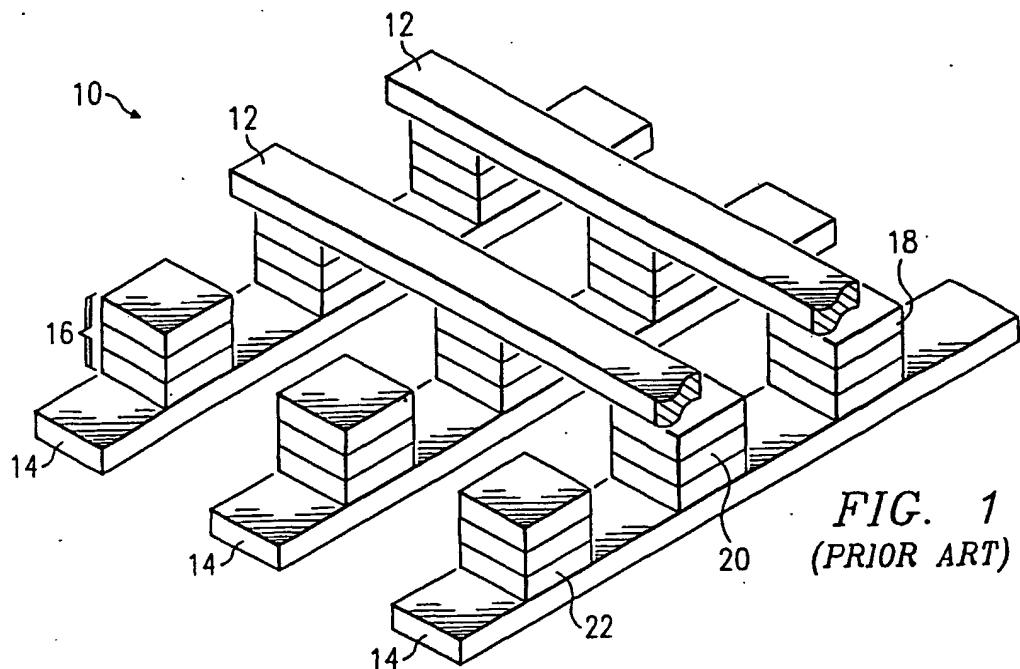
coupling a second logic "0" storage cell having a first end and a second end in series at the first end to the second end of the first logic "0" storage cell; and

coupling the second logic "0" storage cell second end to the second logic "1" storage cell second end.

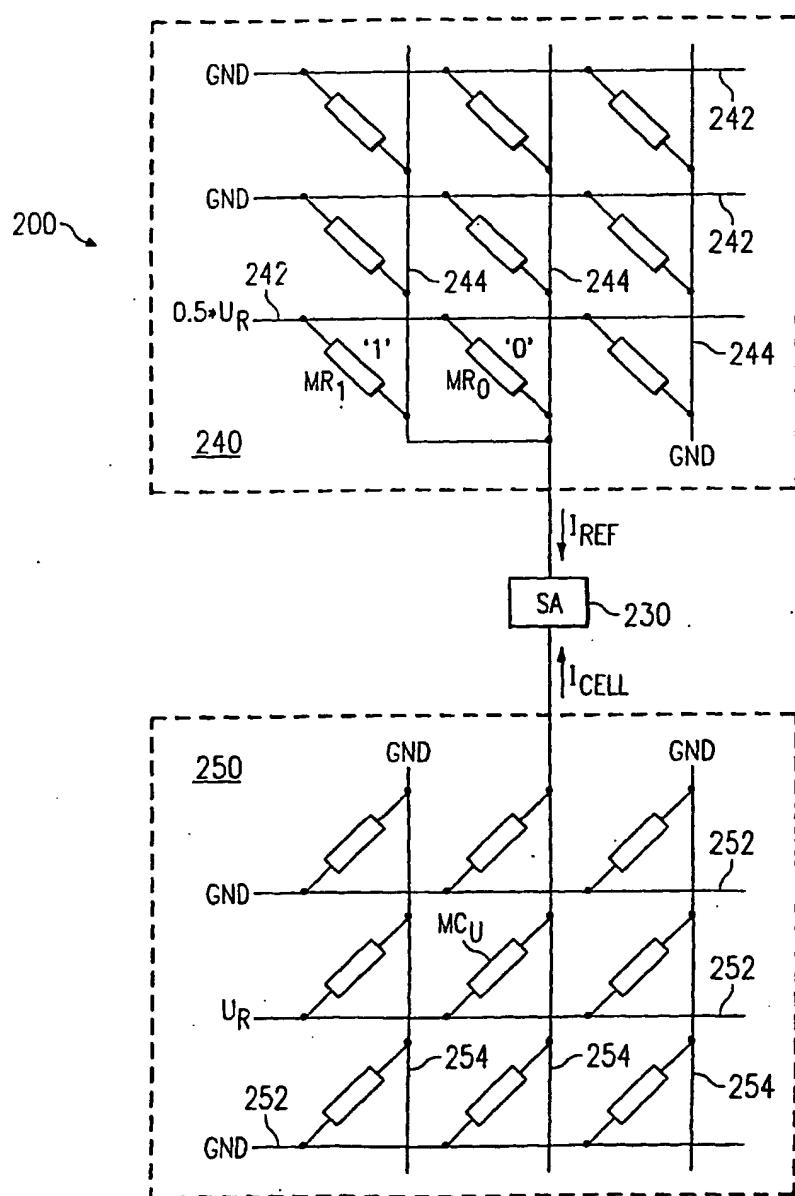
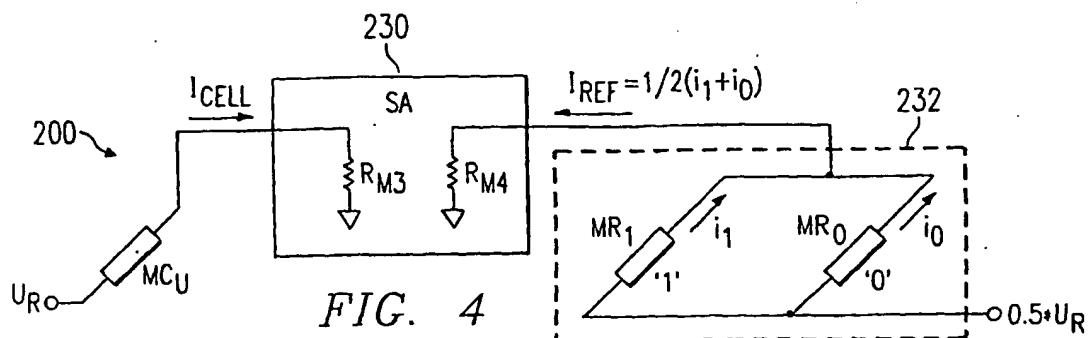
19. The method according to Claim 18, wherein the reference circuit storage cells are part of the MRAM array.

20. The method according to Claim 18, wherein the reference circuit storage cells are part of an MRAM array different from the MRAM array for which the reference current is being generated.

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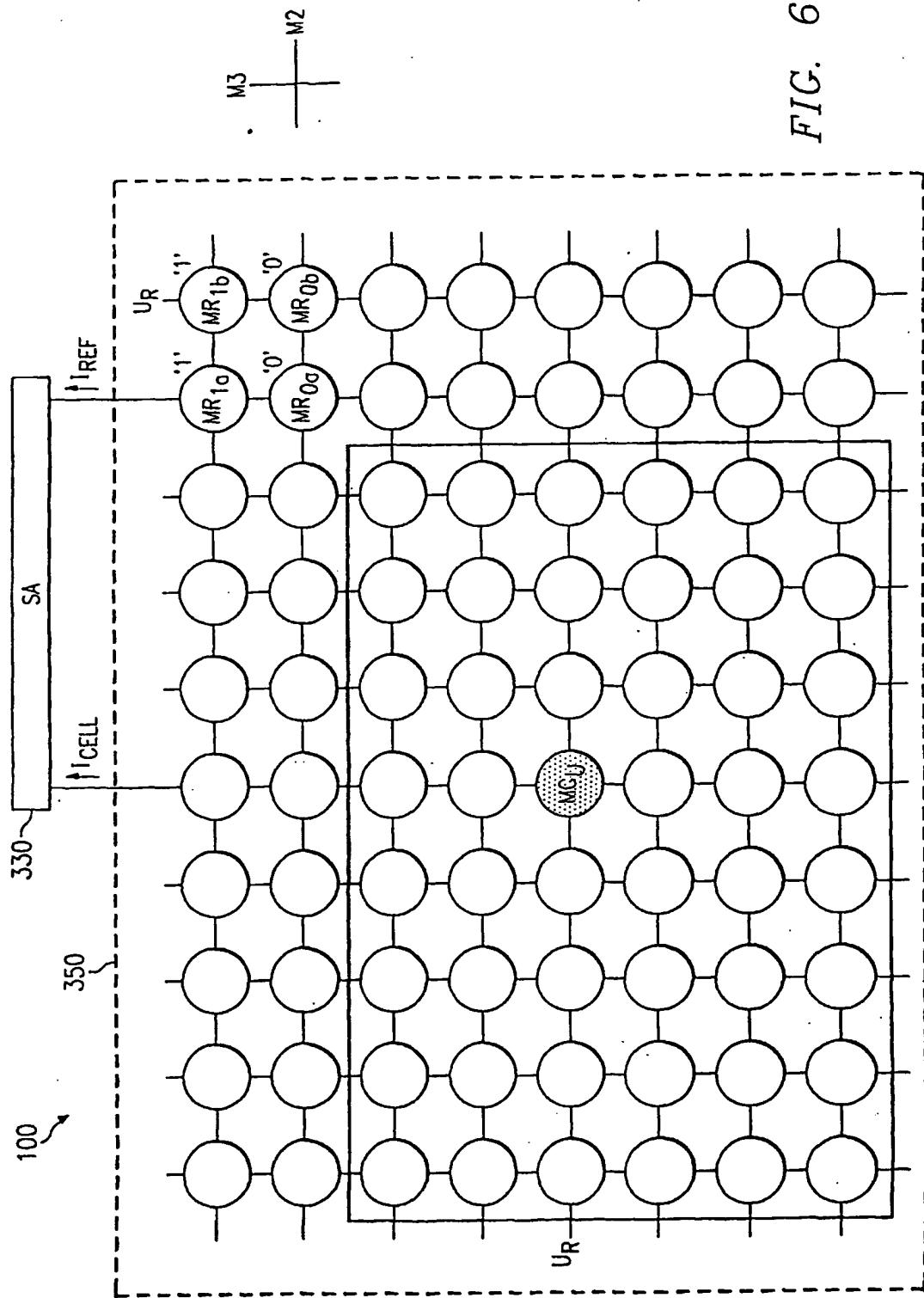


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FIG. 6



(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization  
International Bureau



(43) International Publication Date  
19 September 2002 (19.09.2002)

PCT

(10) International Publication Number  
WO 02/073620 A3

(51) International Patent Classification<sup>7</sup>: G11C 11/16 (74) Agents: BRADEN, Stanton C. et al.; Siemens Corporation - Intellectual Property Dept., 186 Wood Ave. South, Iselin, NJ 08830 (US).

(21) International Application Number: PCT/US02/03040 (81) Designated States (national): CN, JP, KR.

(22) International Filing Date: 24 January 2002 (24.01.2002) (84) Designated States (regional): European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR).

(25) Filing Language: English (26) Publication Language: English

(30) Priority Data:  
60/263,910 24 January 2001 (24.01.2001) US  
09/836,817 17 April 2001 (17.04.2001) US

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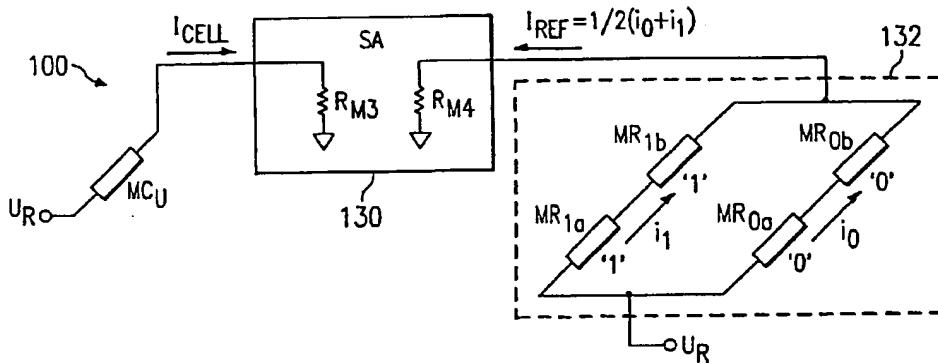
Published:  
— with international search report

(88) Date of publication of the international search report:  
6 November 2003

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: REFERENCE FOR MRAM CELL

WO 02/073620 A3



(57) Abstract: A reference circuit (132) for an MRAM array, including logic "1" reference MRAM cells (MR<sub>1a</sub>) and (MR<sub>1b</sub>) coupled in parallel with logic "0" reference MRAM cells (MR<sub>0a</sub>) and (MR<sub>0b</sub>). The reference current (I<sub>ref</sub>) is coupled to a measurement resistor (R<sub>meas</sub>) of a sense amplifier (130) which is adapted to determine the logic state of an unknown memory cell MC<sub>o</sub>.

## INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 02/03040

A. CLASSIFICATION OF SUBJECT MATTER IPC 7 G11C11/16
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According to International Patent Classification (IPC) or to both national classification and IPC
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B. FIELDS SEARCHED
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Minimum documentation searched (classification system followed by classification symbols) IPC 7 G11C
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Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
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Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
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EPO-Internal, PAJ
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C. DOCUMENTS CONSIDERED TO BE RELEVANT
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Category	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5 608 676 A (MEDLOCK DAVID L ET AL) 4 March 1997 (1997-03-04) column 5, line 64 -column 6, line 58 ---	1-3
E	US 6 501 697 B1 (VAN BROCKLIN ANDREW L ET AL) 31 December 2002 (2002-12-31) column 5, line 29 -column 7, line 56 ---	1,2
P,A	US 6 317 376 B1 (TRAN LUNG T ET AL) 13 November 2001 (2001-11-13) column 2, line 46 -column 4, line 63 ---	1,2

Further documents are listed in the continuation of box C.

Patent family members are listed in annex.

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Date of the actual completion of the International search
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11 June 2003
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Date of mailing of the International search report
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Degraeve, L
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on patent family members

International application No	PCT/US 02/03040
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